Development and operation of electronics for the Belle II Central Drift Chamber

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Belle II @ SuperKEKB

- asymmetric e^+-e^- collider ($\sqrt{s}$ = 10.58 GeV)
  - $e^+e^- \rightarrow \Upsilon(4S) \rightarrow B\overline{B}$
- A wide range of physics goals

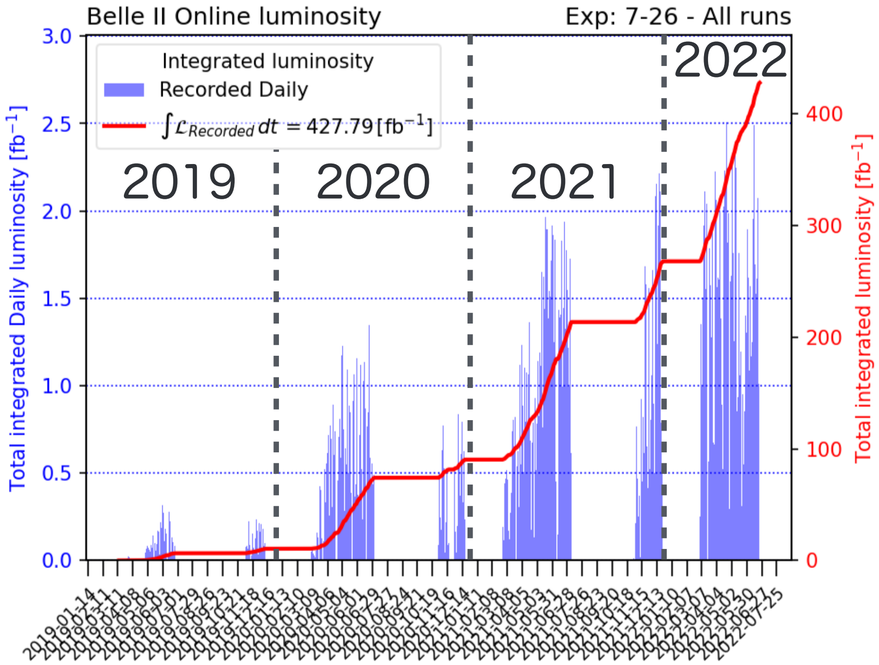
  B meson: Time-Dependent CP asymmetry

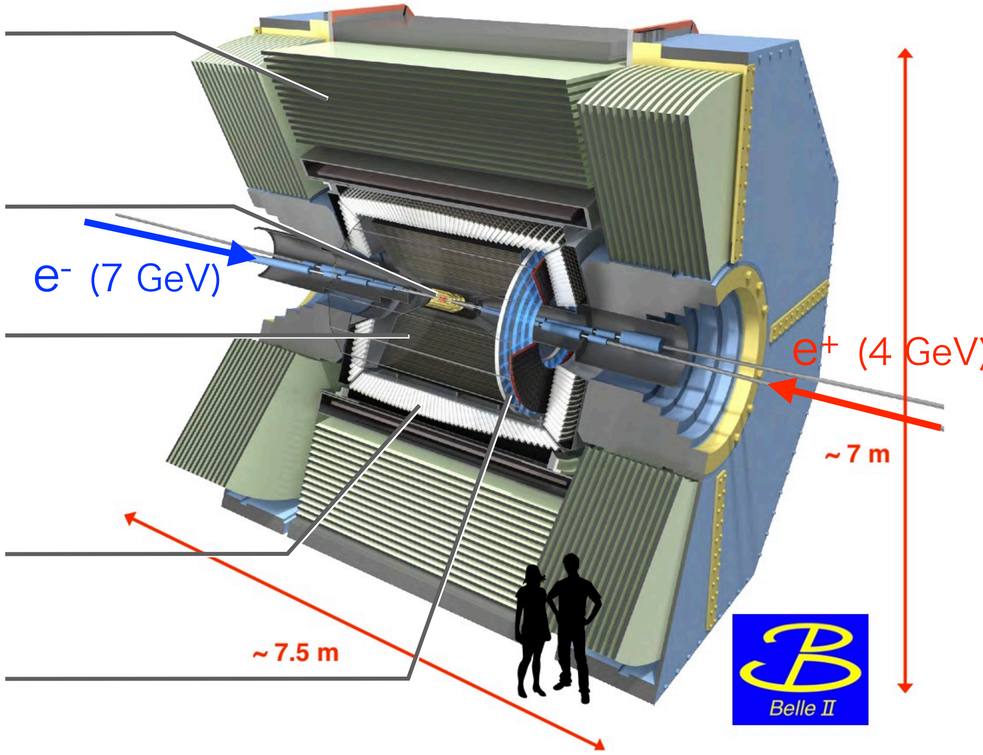
  tau: Lepton Universality, Lepton Flavor Violation

  etc..

Luminosity	Design	Accomplished
Integrated	50 /ab (Belle x50)	428 /fb
Peak	6.5 x 10^{35} /cm^2/s	4.7 x 10^{34} /cm^2/s

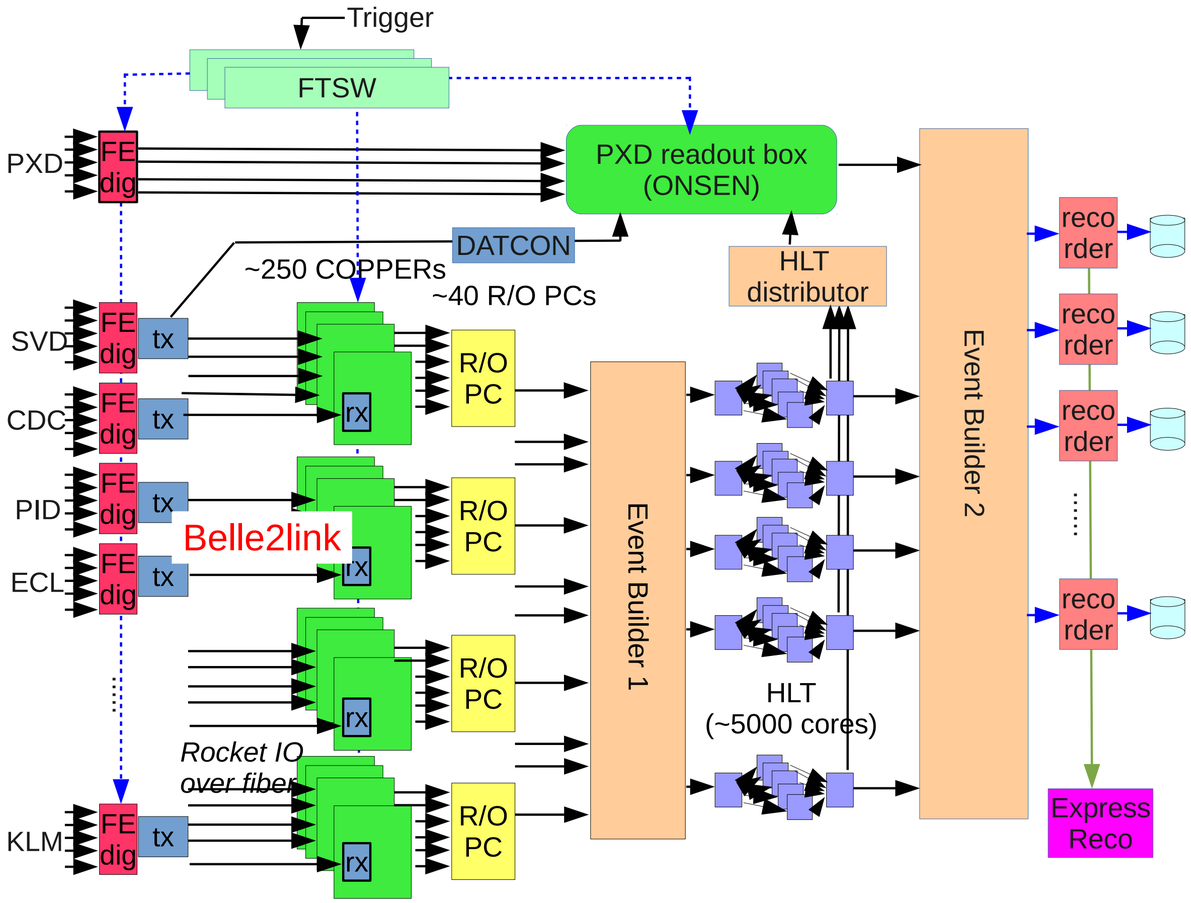
World Record!!

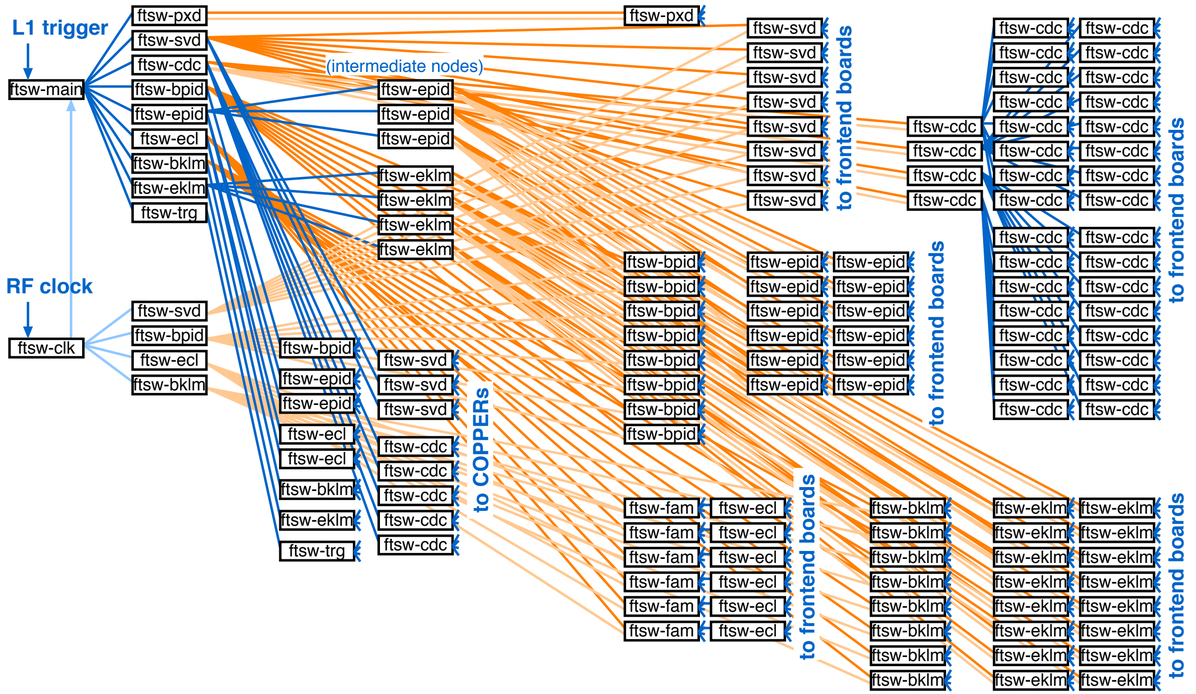




Belle II Trigger & DAQ system

In this presentation, we will focus on the front-end (FE) modules of CDC.





CDC Trigger & DAQ sytem

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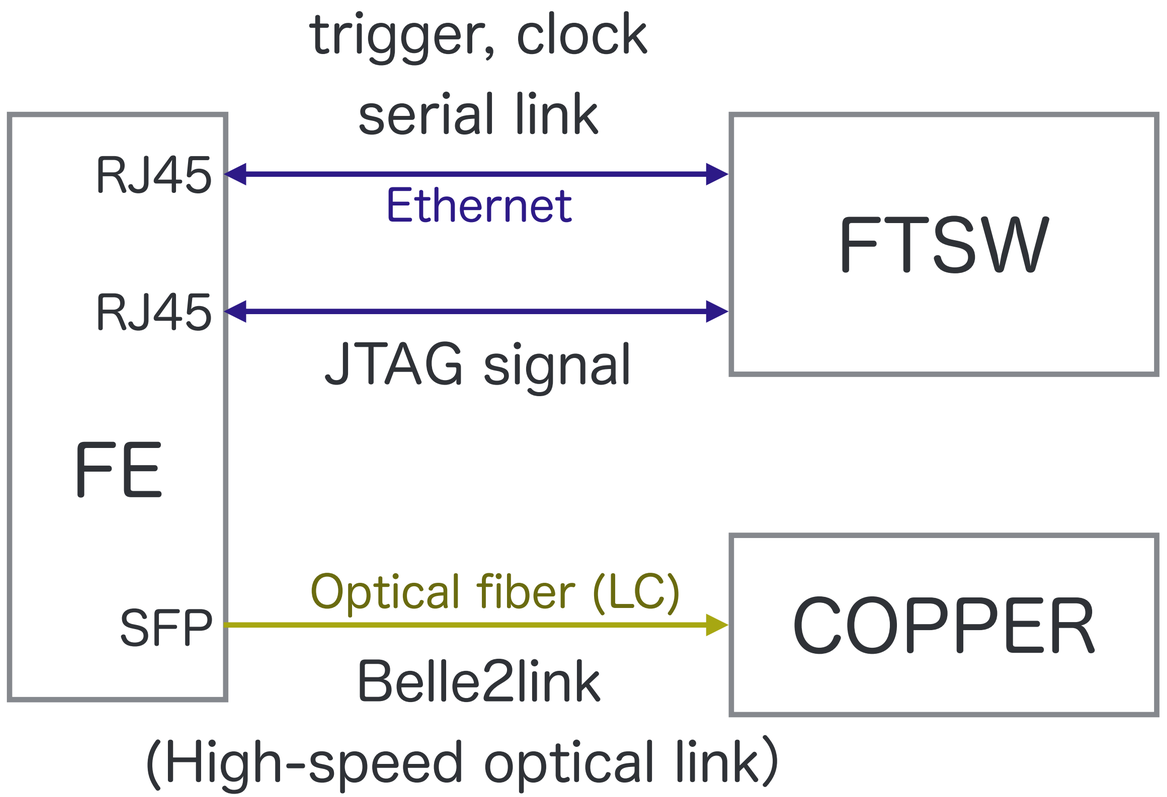
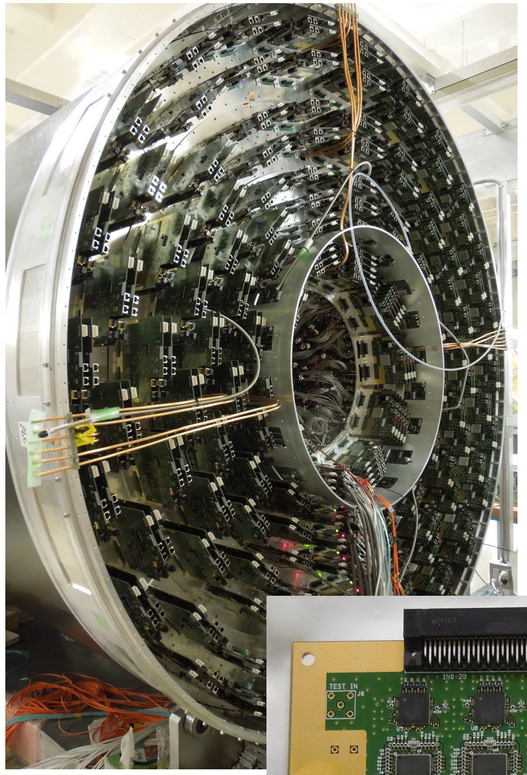
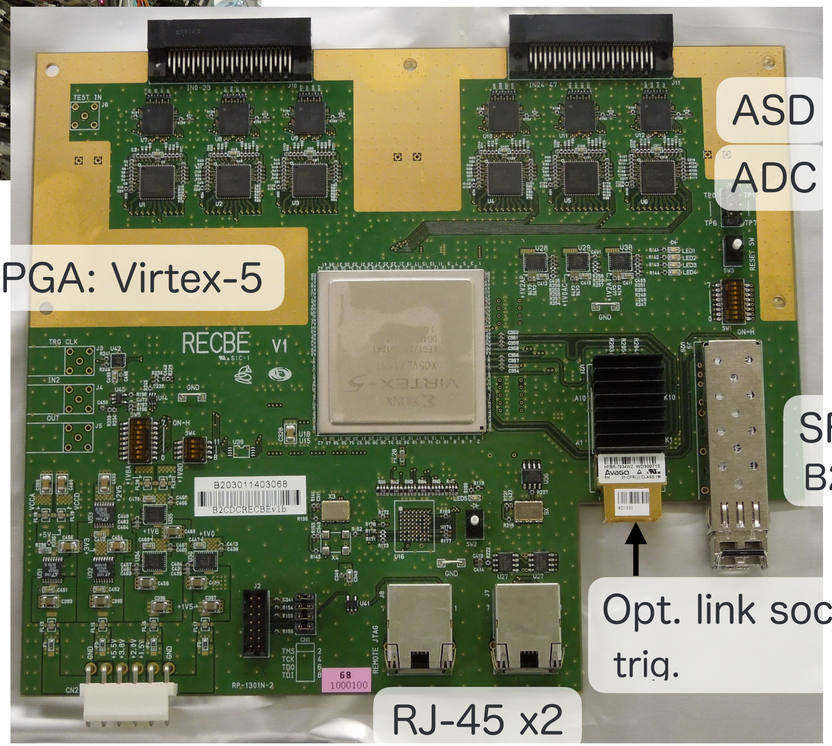


- CDC FE module
  - Digitize signals from the detector using FPGA
    - Field-Programmable Gate Array: FPGA
  - 300 FE modules
- Front-end Timing Switch: FTSW
  - FPGA-based digital signal processing
  - 254 Mbps serial link (B2TT)
    [to FE] Distribution of triggers and commands
    [from FE] Monitoring the FE status
  - JTAG signals : FPGA configuration
- Common platform for FE readout : COPPER
  - Collect digitized detector data using Belle2link

CDC front-end module

- Roles
  - Amplify, shape, and digitize CDC electrical signals
    - Amp. Shaper Discriminator: ASD
    - Part of the data used for triggering
  - Receive trigger and transfer event data
- Radiation countermeasures
  - For long-term operation, we have implemented countermeasures against radiation damage.
  - Evaluation of radiation tolerance of ICs by irradiating neutrons and gamma rays
    - Regulator, DAC, ADC, SFP etc..
  - Implementation of self-repairing functions for soft errors on FPGAs.
  - Previous studies : 14th B2GM, 10.1088/1748-0221/7/02/c02022, 10.1016/j.nima.2018.10.130, 10.1016/j.nima.2019.163247





DAQ efficiency (Mar.-Jun. in 2022)

Physics-run time

Category	Ratio
Running	92.6%
Belle II trouble	3.4%
DAQ Stop-to-Start	3.0%
HV ramp-up/down	0.8%
HV trip or error	0.2%

DAQ dead-time during runs

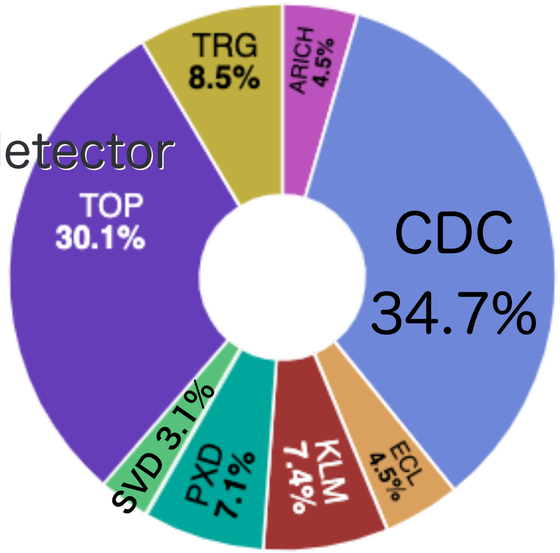
Category	Ratio
Live time	94.1%
Injection veto	5.2%
others	0.7%

DAQ efficiency : 87.1%

(target : 90%)

PID detector

run-stop ratio



Causes of “Belle II trouble” and “DAQ Stop-to-Start”

The beam intensity will increase. (x10)

→ To maintain and improve DAQ efficiency, electronics’s radiation resistance is crucial!!

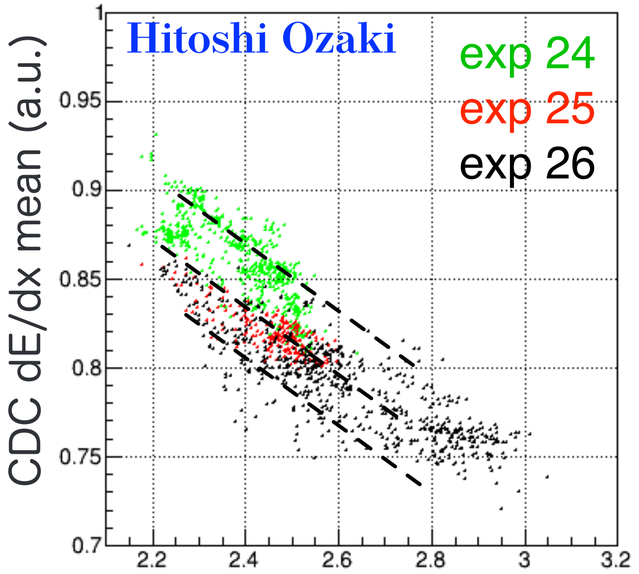
CDC is affected by beam backgrounds

Beam background

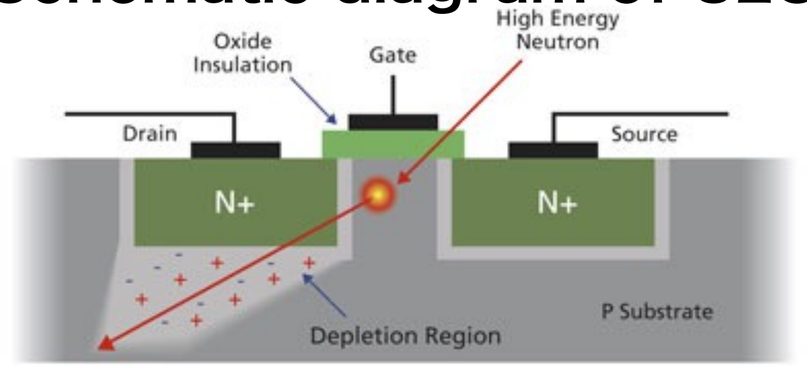
- electron, photon, neutron ...
- Higher hit occupancy, gas gain drop, and so on..

especially, Neutron-induced soft errors in an FPGA

- Process:
  - A charged particle can be generated due to the neutron-nuclear interaction in a semiconductor.
  - This particle creates electron-hole pairs that affect FPGA logic.
- Single Event Upset: SEU
  - not permanent damage
  - should be fixed by auto-recovery schemes or re-configuring the FPGA.
- Neutrons at Belle II: 10^{12} n/cm^2 for 10 years

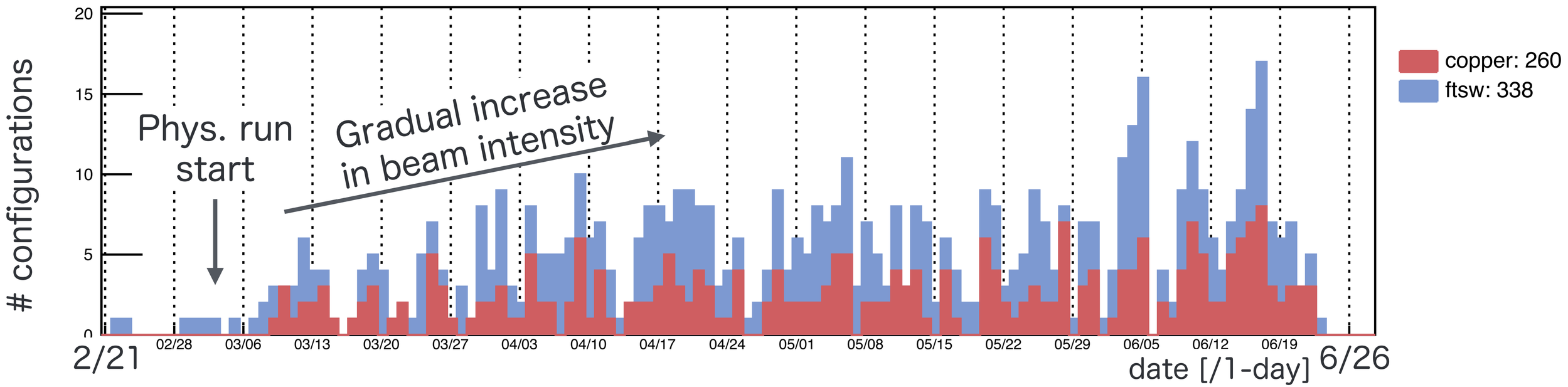


Schematic diagram of SEU

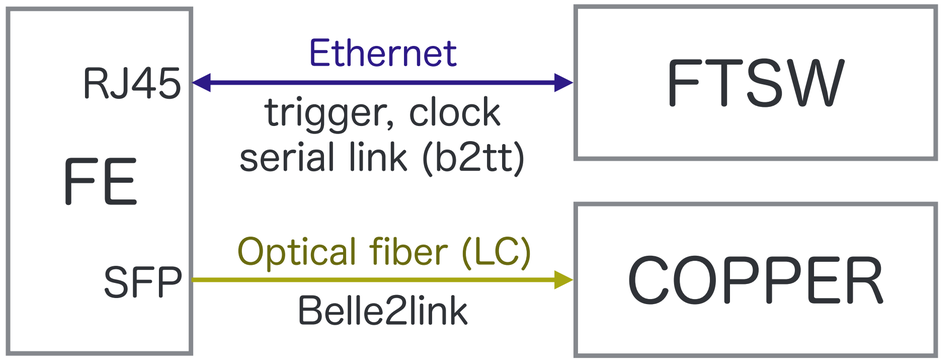


ref. Cosmic rays damage automotive electronics, http://www.embedded.com/print/4011077

Errors during the 2022 run

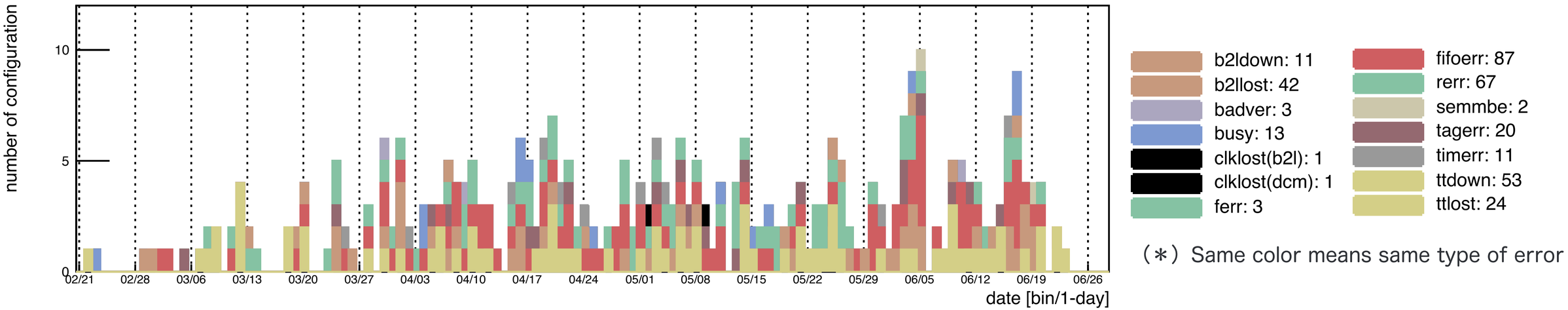


It is rare for many FEs to be in an abnormal state simultaneously.



- Error on COPPER
  - Checking for damage in data from FE
  - Header mismatch or missing data, etc..
- Error on FTSW
  - It depends on the state of the FE when read out through the serial link, and there are multiple types. → Next page for more details

Errors during the 2022 run: FTSW



(*) Same color means same type of error

Type of errors

FIFO error : 87

FIFO for storing trigger info. is full.

Mainly due to Belle2link failure

FTSW link (tt) disconnected : 77

Buffer full or Clock instability : 70

Belle2link (b2l) disconnected : 53

event tag/timing error : 31

Mismatch between trigger info. and values calculated inside FE.

Busy : 13

Data transfer is stuck with Belle2link

others : 7

Not seeing many radiation-induced SEUs?

Many communication-related errors

→ Main cause may be elec. noise due to accelerator operation or beam backgrounds?

SEU Auto-recovery scheme : SEU Controller

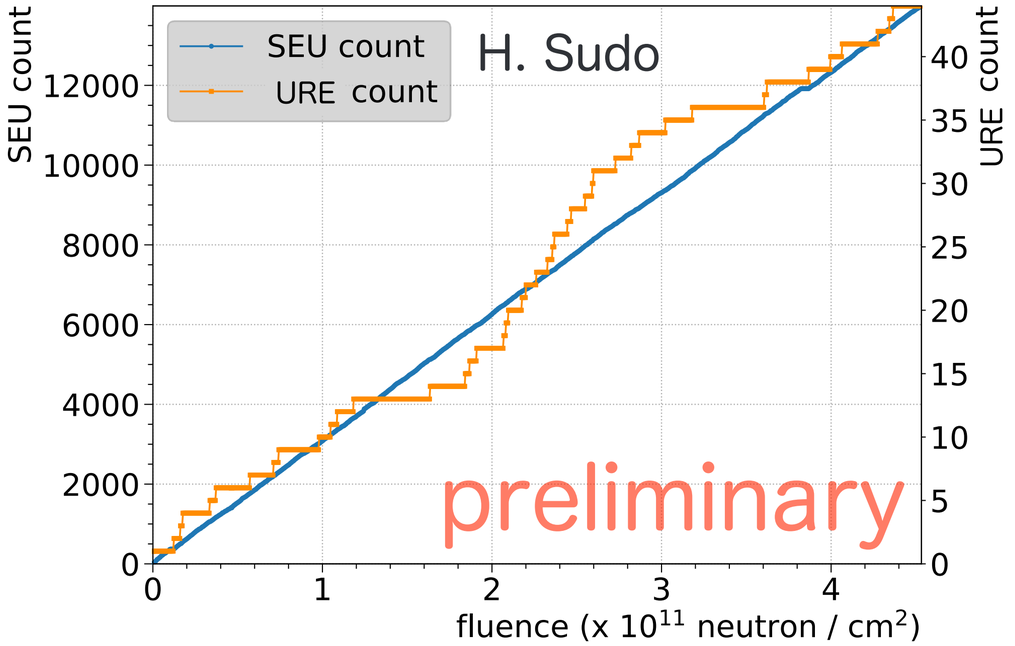
- SEU Controller
  - Checking for errors in each frame with two methods
    - 164 Bytes as 1 Frame
    - Error Correction Code, Cycle Redundancy Check
  - Xilinx Inc. distributes a higher-performance library called Soft Error Mitigation (SEM) for successors to Virtex-5

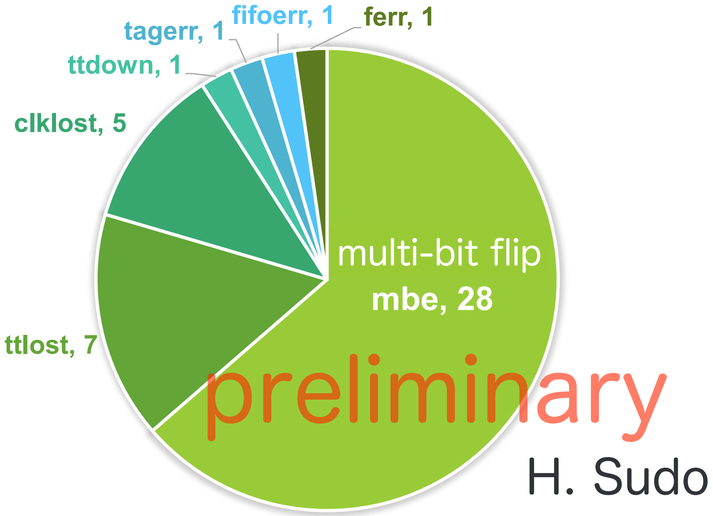
bitflip [bit]	Behavior
1	correction
2	non-correctable, detection only
>3	unstable

- Implemented but not functioning properly.. no protection against neutrons
  - Symptoms : SEU Controller initialization does not finish, so nothing starts
  - Works properly when configured from the manufacturer's (Xilinx) software.
  - FTSW seems to be unable to accurately emulate JTAG signals or the configuration scheme.
    → In config., the final reset sequence required to start normal operation was missing. Fixed

SEU Controller: Functionality check

- Neutron irradiation tests were performed.
  - TANDEM accelerator at Kobe University, Japan
  - ~2 MeV neutrons using a 3-MeV deuteron beam and a Be target
  - Total fluence: 4.5 x 10^{11} n/cm^2
- SEU Controller successfully detects and corrects SEUs.
  - SEU rate: 3.1 x 10^{-8} SEU/(neutron/cm^2)
  - URE rate: 1.0 x 10^{-10} URE/(neutron/cm^2)
    - UnRecoverable Error: URE
    - includes multi-bit flips and all the FTSW errors
    - requires FPGA re-configuration to fix.





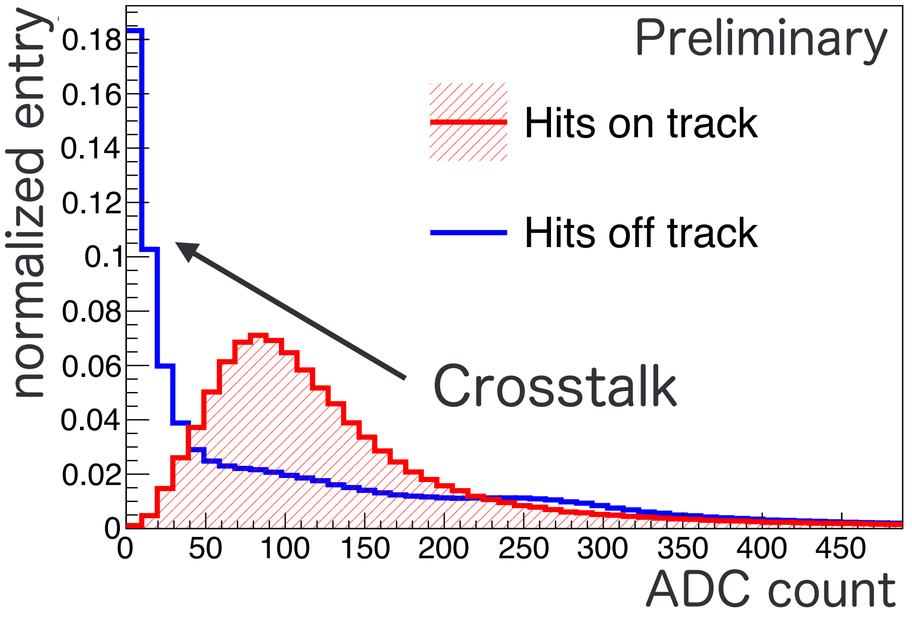
We plan to investigate whether the errors in the past physics runs are caused by neutrons in more detail.

Purpose and Progress of the upgrade plan

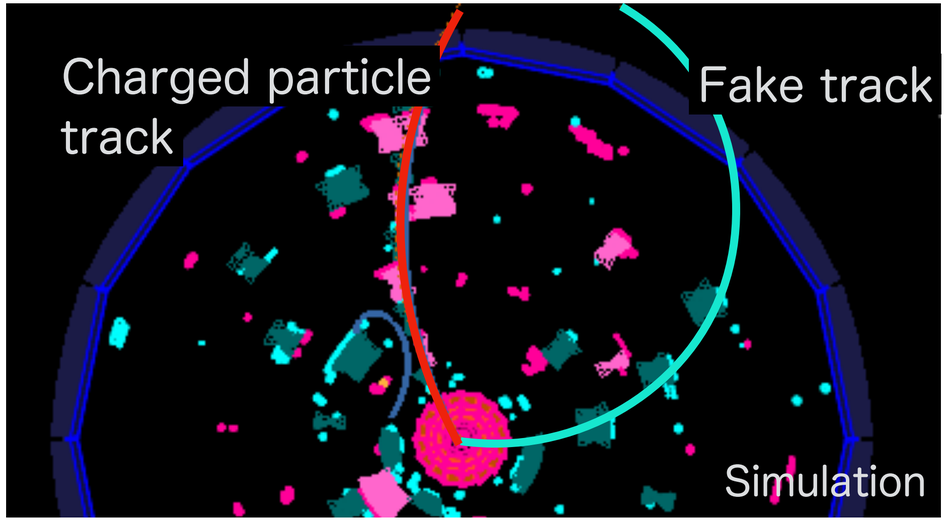
- Reduction of crosstalk effects
  = a signal on one wire in an ASIC affects another wire
  - has a significant impact on the increase of fake tracks with the improvement of luminosity
    ⇒ especially in degrading trigger performance

- Improvement of radiation resistance
  - The current optical modules are permanently damaged at around 300 Gy
  - Requirement: 1 kGy for 10-year operation
  - We already found several candidates of rad-hard QSFPs

Development of a new ASIC & 1st prototype production

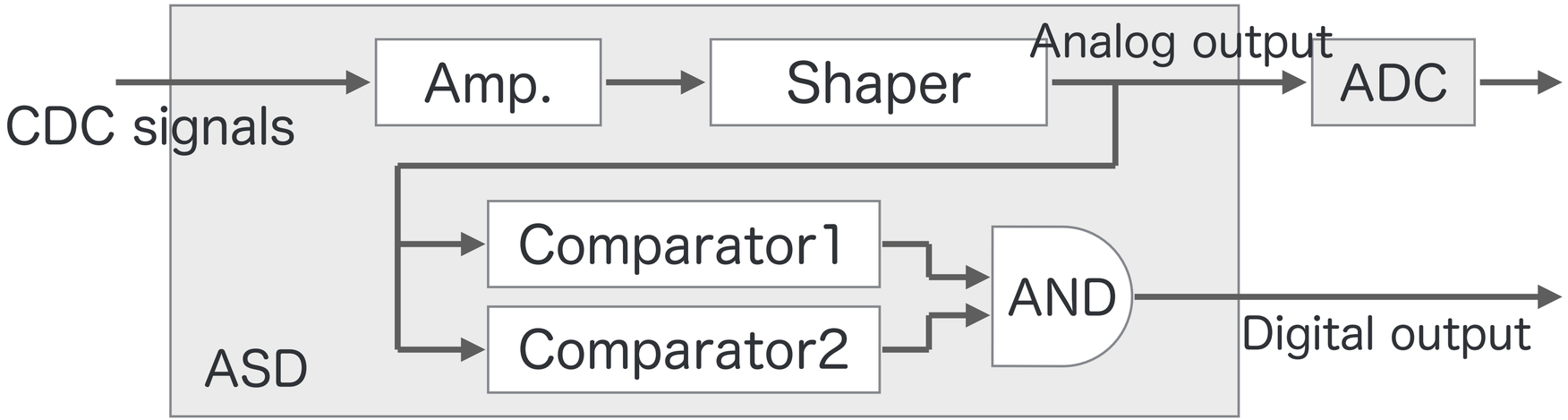


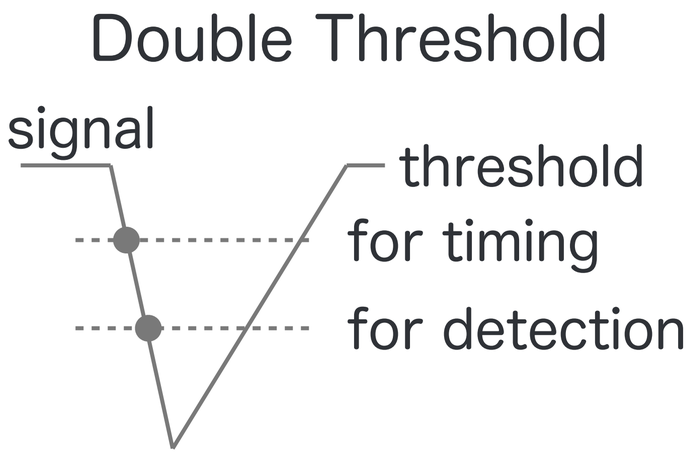
Fake tracks due to crosstalk



New ASIC: RAPID

Developed by Miyahara (KEK)





- ASD and ADC in one chip (8 ch/chip)
- Double Threshold scheme
  - Reducing the crosstalk effect
- ADC : 10 bit, 2 Vp-p, Comp. : 10 bit, 3 Vp-p

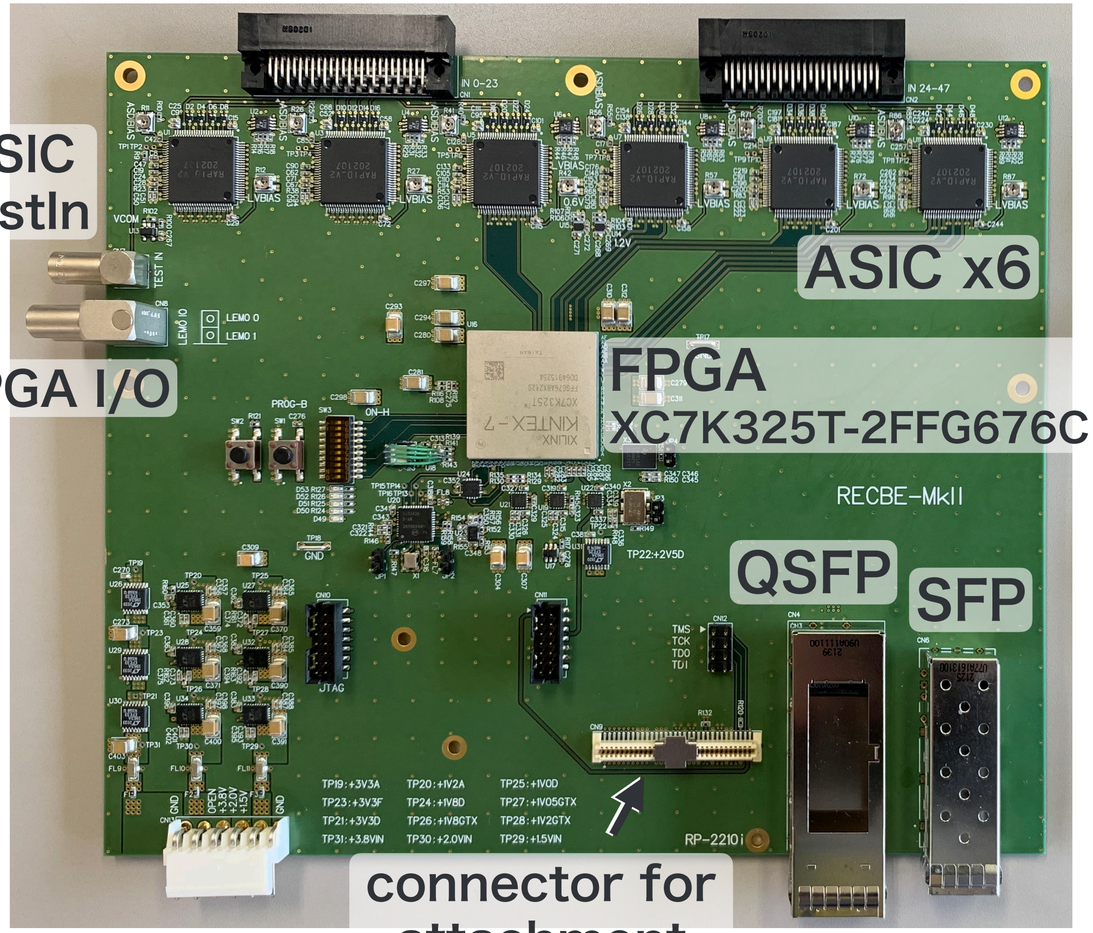
Others

- ~100-MSPS ADC operation at maximum.
- Adjustable R and C in Amp. · Shaper, Adjustable gain in ADC

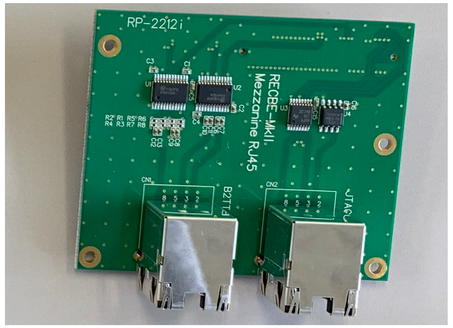
	Current V.	New ASIC
Gain [V/pC]	(analog) 1.1, (digital) 7	0.9
Gain linearity [pC]	0.4	1.1
ADC sampling [MSPS]	31.25	63.5
Crosstalk [mV/pC]	14	1.0
Power usage (ASD+ADC) [mW/ch]	134	41.3

Changing from single-end to differential wiring strongly reduces the crosstalk level.

New Readout Electronics: 1st prototype



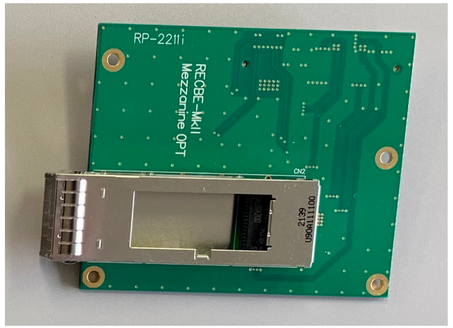
Two attachment boards



Current operation

RJ45 : trigger and clock receive

RJ45 : FPGA configuration



New operation idea

2 lanes : trigger and clock receive

1 lane : FPGA configuration

<u>QSFP</u>

1 lane : data acquisition (2.54 Gbps/lane)

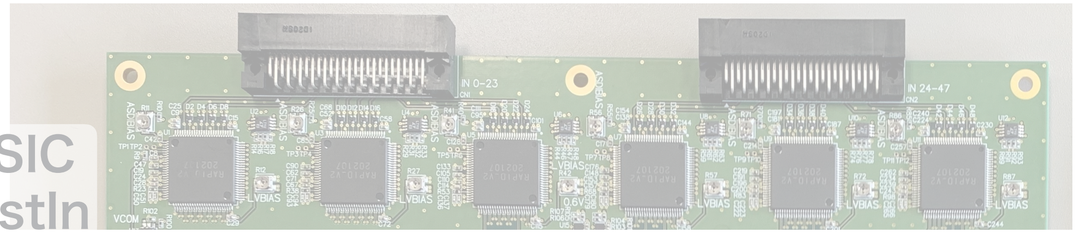
2 lanes : trigger data transfer (10 Gbps/lane)

<u>SFP</u>

Dedicated for testing and will be removed

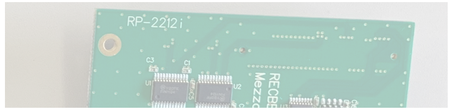
Used for data acquisition in evaluation tests

New Readout Electronics: 1st prototype



ASIC
TestIn

Two attachment boards



Current operation

Testing the functionalities and checking the performance.

We will report results in coming workshops.

connector for attachment

QSFP

1 lane : data acquisition (2.54 Gbps/lane)

2 lanes : trigger data transfer (10 Gbps/lane)

SFP

Dedicated for testing and will be removed

Used for data acquisition in evaluation tests

Summary

- SuperKEKB is steadily increasing beam current and luminosity.
- While the impact of radiation is increasing, it is important to minimize dead time in data acquisition with the Belle II detector.
- We are identifying and addressing issues through operation and making improvements and updates.
- Upgrades to the readout module have also started for long-term operation.

Backup

CDC FE (RECBE)

Amp Shaper Discriminator (ASD)

- Analog out: waveform
- Digital (discriminator) out: hit timing

Analog-to-Digital Converter (ADC)

- 2 Vp-p, 10 bit
- 31.25 Mbps?

Field-Programmable Gate Array (FPGA)

- Virtex5 (xc5vlx155t)
- Data processing

Optical module from Avago

- CDCTRG

Small Form-factor Pluggable (SFP)

- Belle II link (b2l)

RJ45

- Belle II trigger timing (b2tt)
- Firmware (fw) download