Australian Government

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STAR Tandetron 2MV Accelerator

High Voltage Generator repair and modernisation.

Centre for Accelerator Science

Accelerator Systems Development

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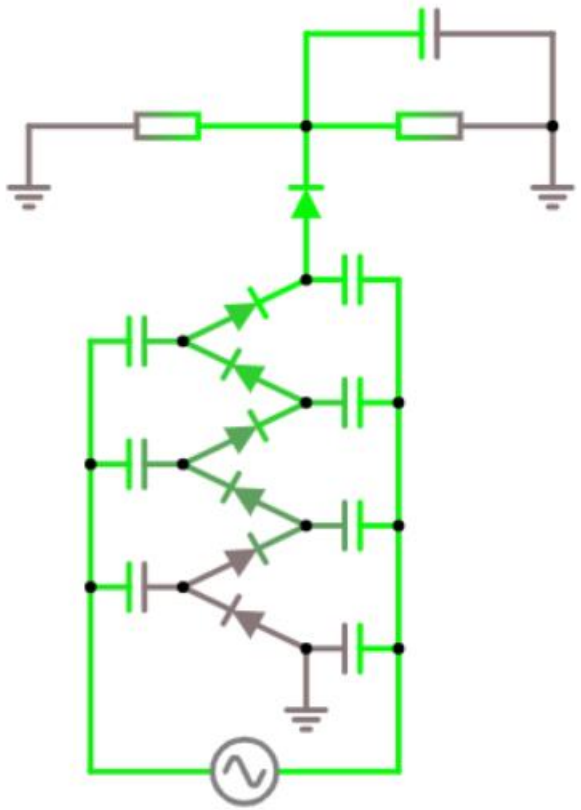
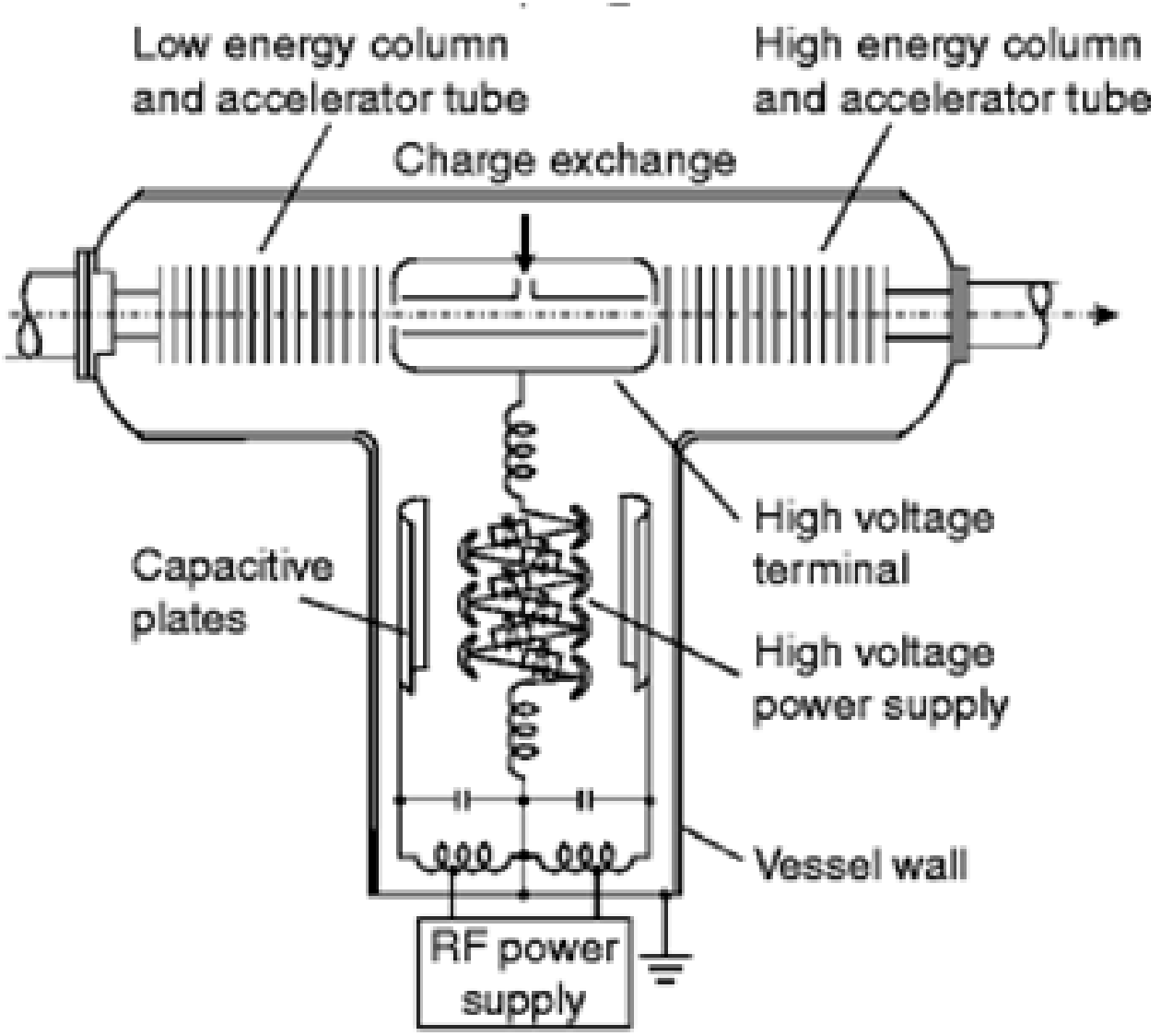
Accelerator Introduction

- Manufactured by High Voltage Engineering Europa (HVEE)
- Online in 2003
- 2 Million Volts – Terminal voltage
- Alpha, Proton and SNICS Ion Sources
- AMS and IBA end stations

Accelerator Introduction

- STAR Tandetron 2MV Accelerator
  - Solid state voltage multiplier used instead of a belt or pellet chain.





Role of Inverter PCB

- Matching the resonant frequency of the voltage multiplier for higher efficiency
- Controlling the power output through Pulse Width Modulation
- Implementing system safety and interlocks

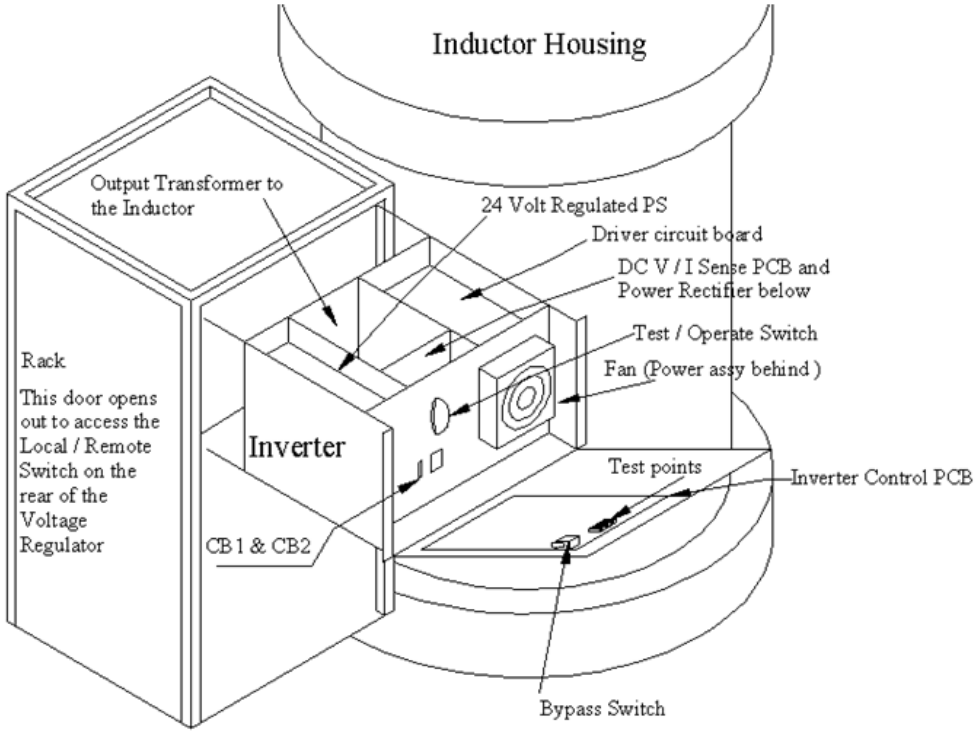
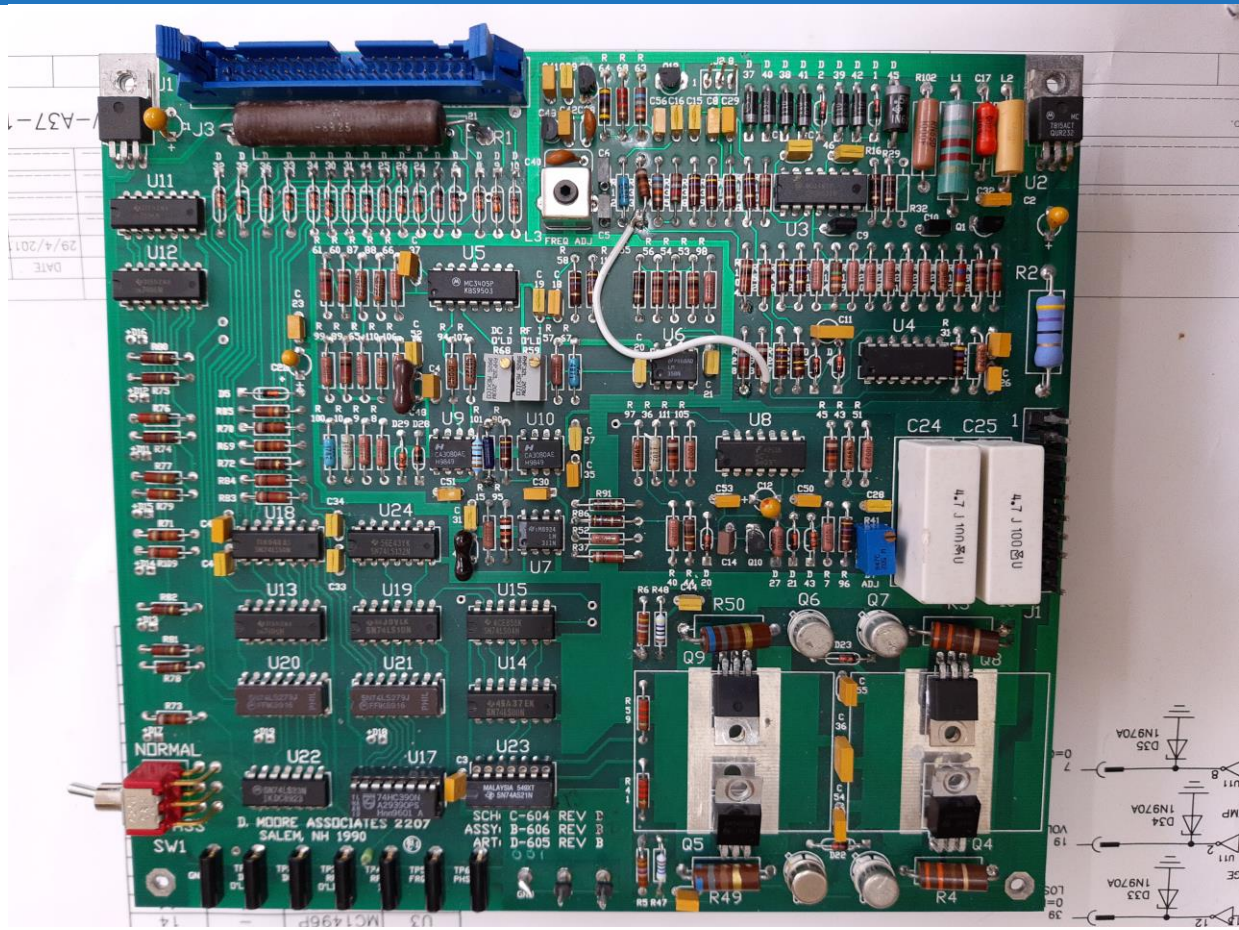


Fig 10 General Arrangement of the Inverter

Issues

- Damaged Inverter PCB
  - Very impressive but complicated design
  - Made with analogue ICs and discrete components
    - Obsolete components unavailable
    - Direct substitutes unavailable.



Current status of Inverter PCB

- Lower efficiency.
  - Driving frequency is currently through an external generated.
  - Operation is at a fixed frequency.

- IGBT ‘Half bridge’
  - IGBT used to replace obsolete and unavailable BJTs.

- The risk with *‘Temporary Fixes’* are that they almost always become permanent fixes.

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Repair and upgrade options

1. Purchase a modern replacement driver from the manufacturer (HVEE)
2. Try and source the obsolete parts for a one time fix.
3. Redesign control system
    a) New analogue PCB with currently available components.
    b) Implement a PLC replacement

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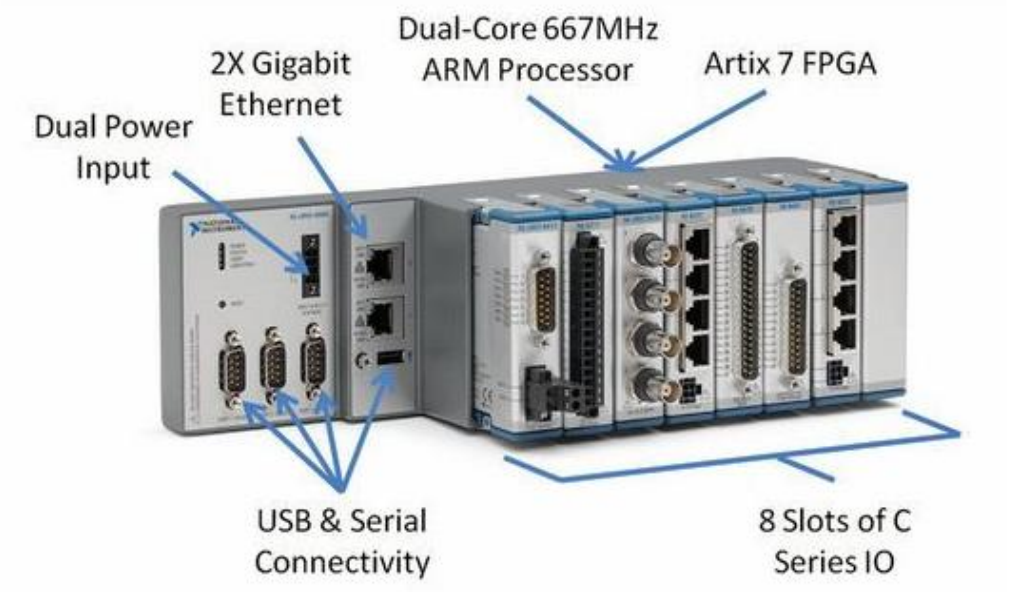
Proposed hardware & software: PLC Implementation

- Hardware
  - NI – Compact RIO (cRIO9035) chosen to use as test bed
    - Using LabVIEW 2019
  - Digital & Analogue I/O Cards
    - FPGA on Processor die.
    - C Series I/O cards used
      - Standard digital cards lacked adequate speed and precision
      - High speed digital card required for 41 kHz (Why?).
- Software
  - Phase Locked Loop (40-42kHz)
    - Issues - process delay and jitter
    - Required streamlining code and parallel synchronisation
  - Pulse width modulation and pulse overlap prevention
    - Duty cycle of between 3% and 35 % for 50 kV to 2 MV on terminal
    - Very tight coding required to achieve correct duty cycle for PWM



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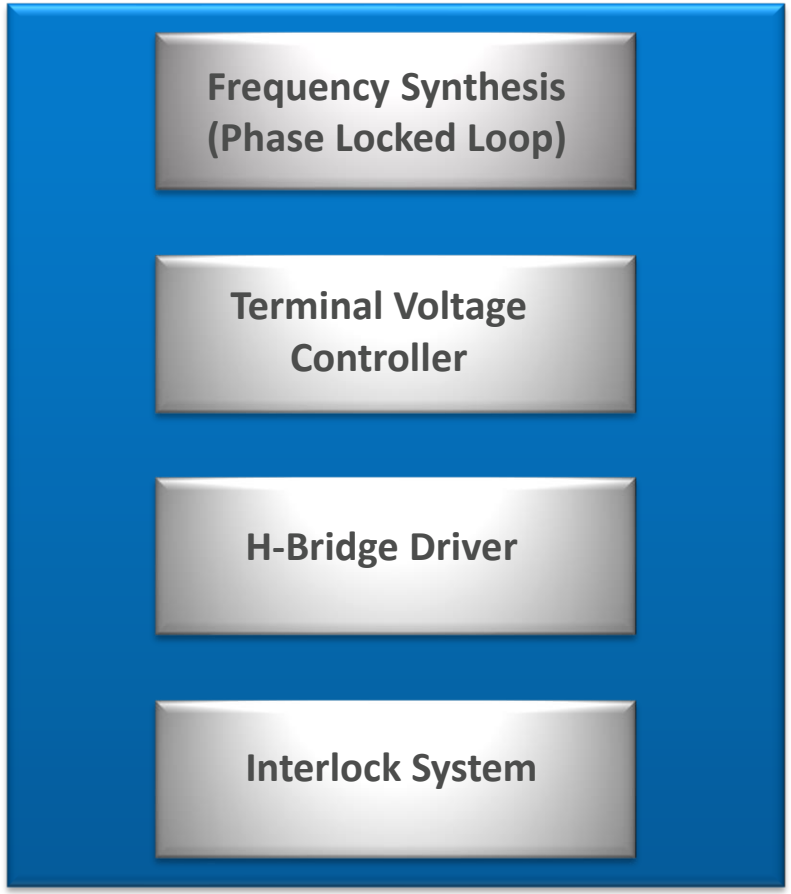
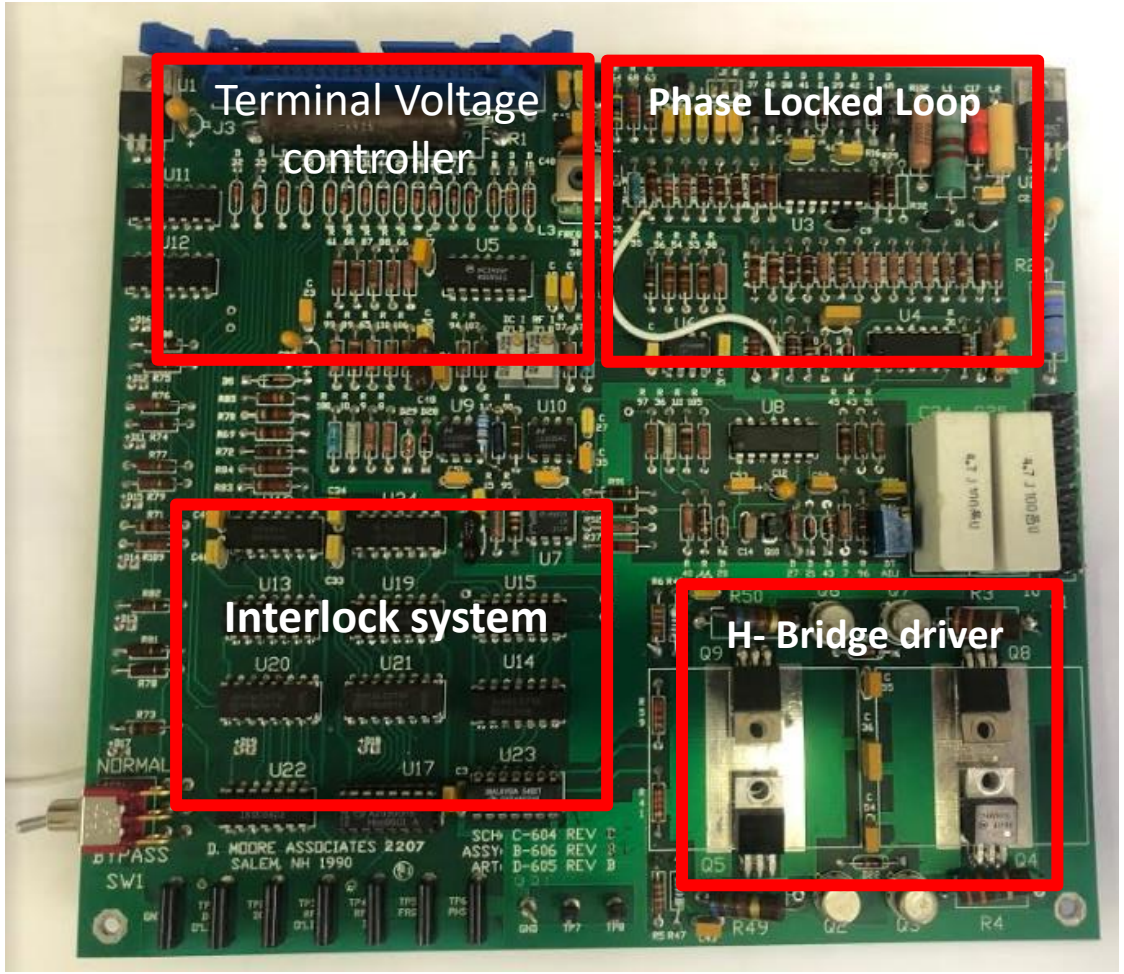
PLC control system requirements



NI cRIO control system



HVEE board

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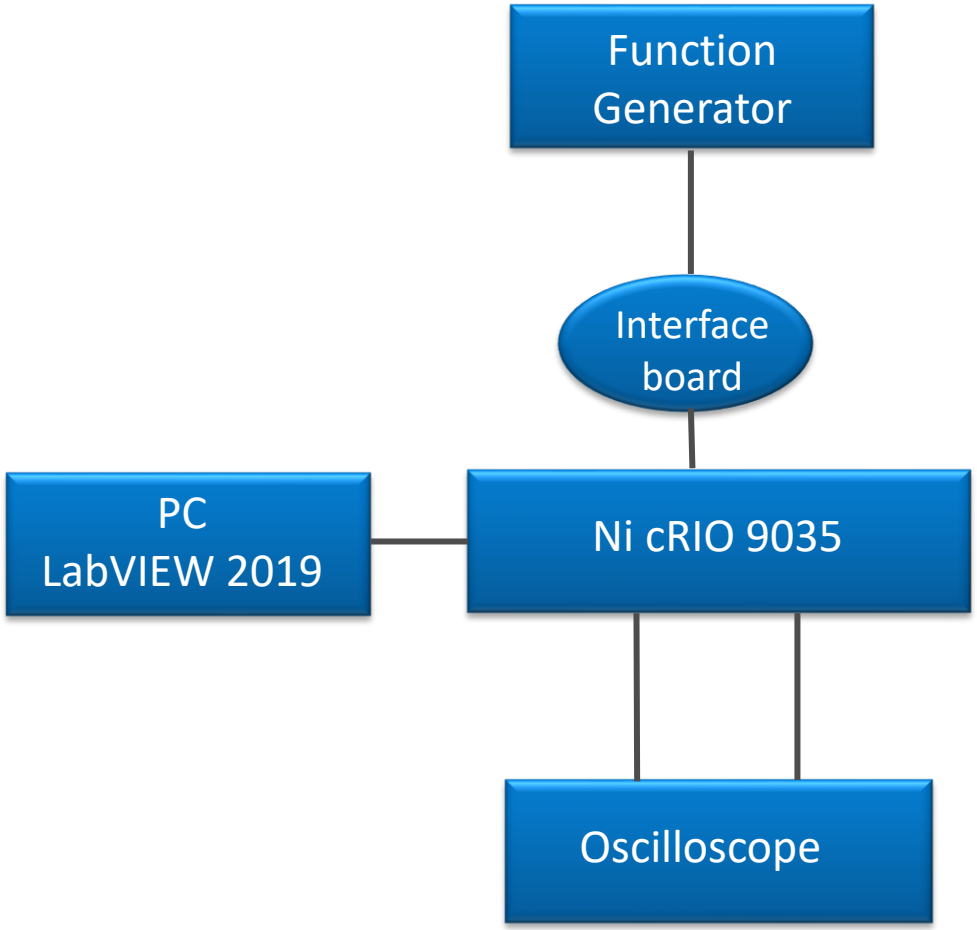
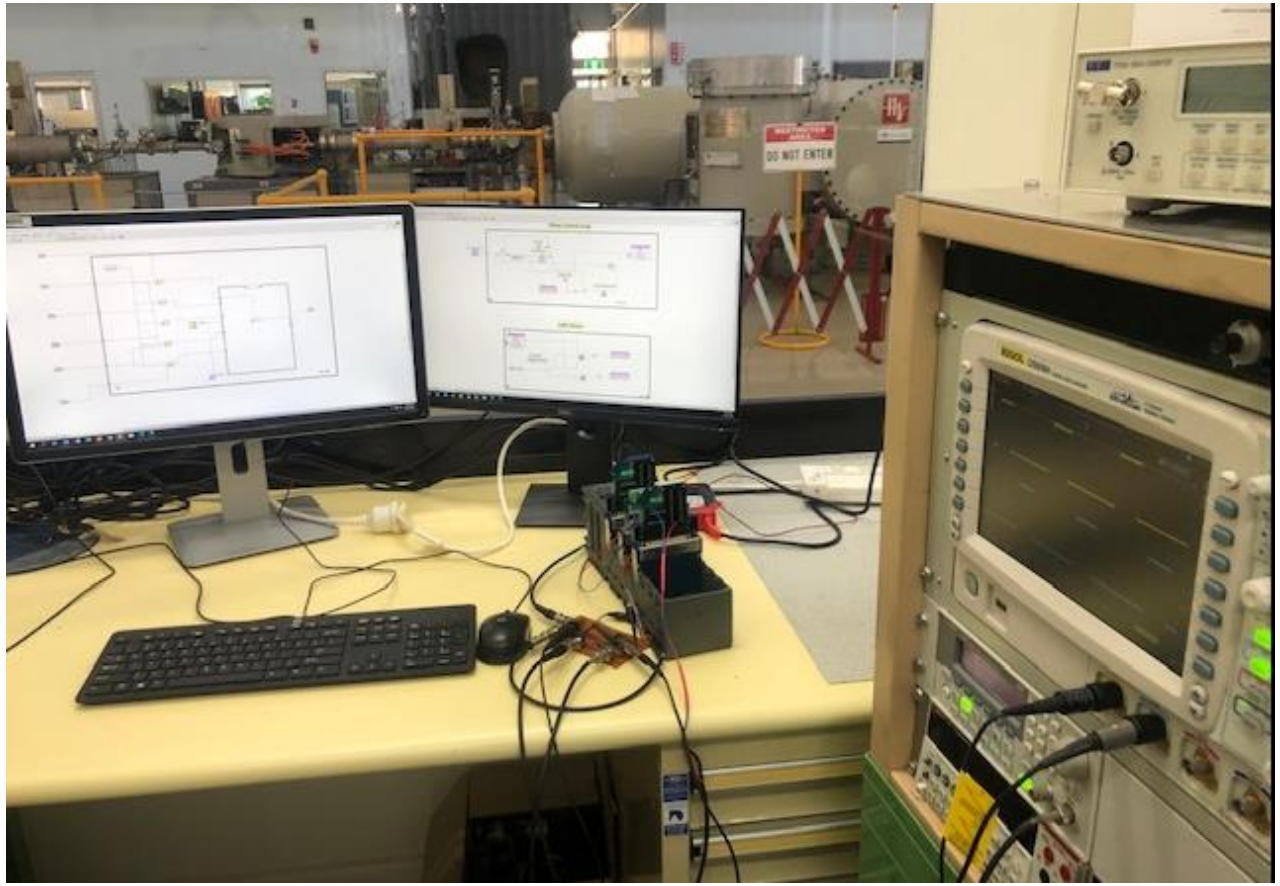
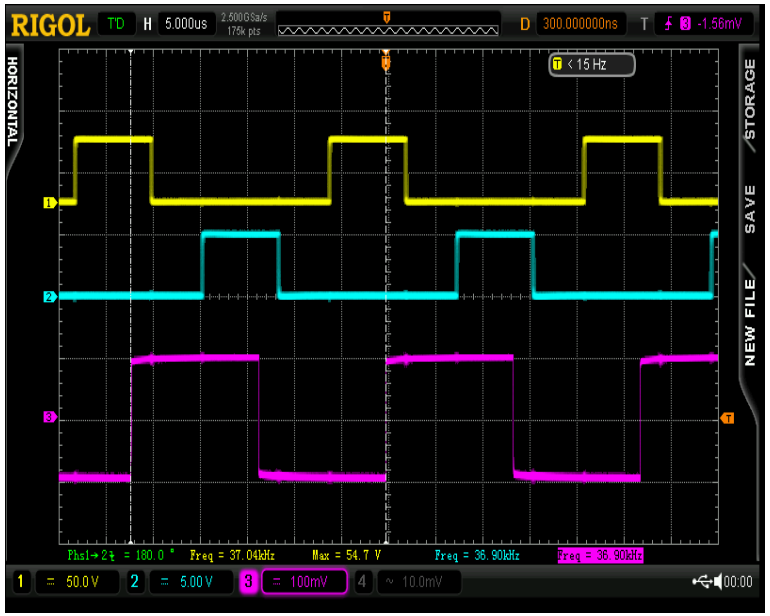
Laboratory setup

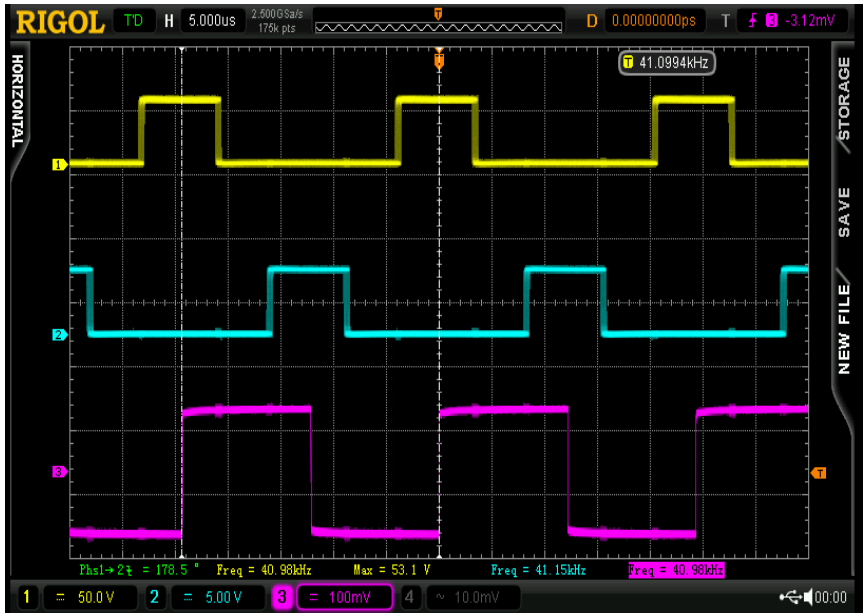




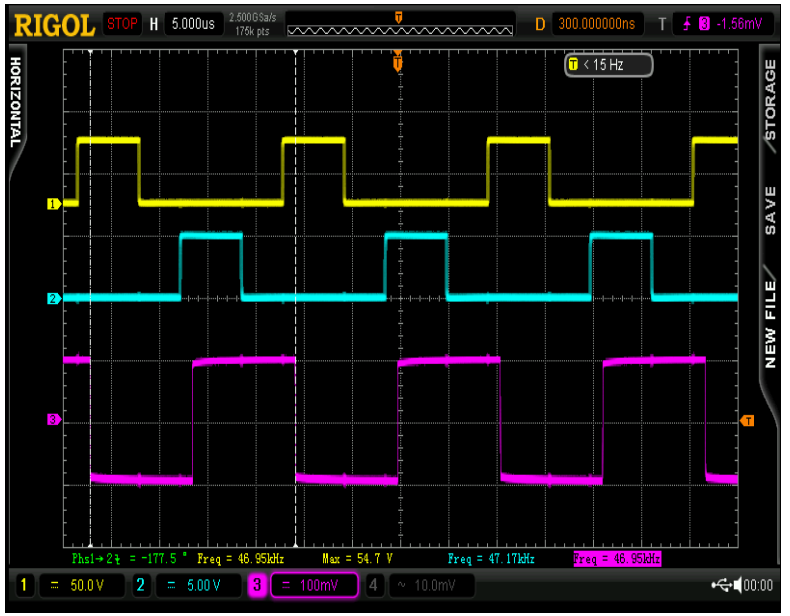
Measurement results: Frequency matching



Frequency : 37 kHz
Duty Cycle: 30%



Frequency : 41 kHz
Duty Cycle: 30%



Frequency : 47 KHz
Duty Cycle: 30%

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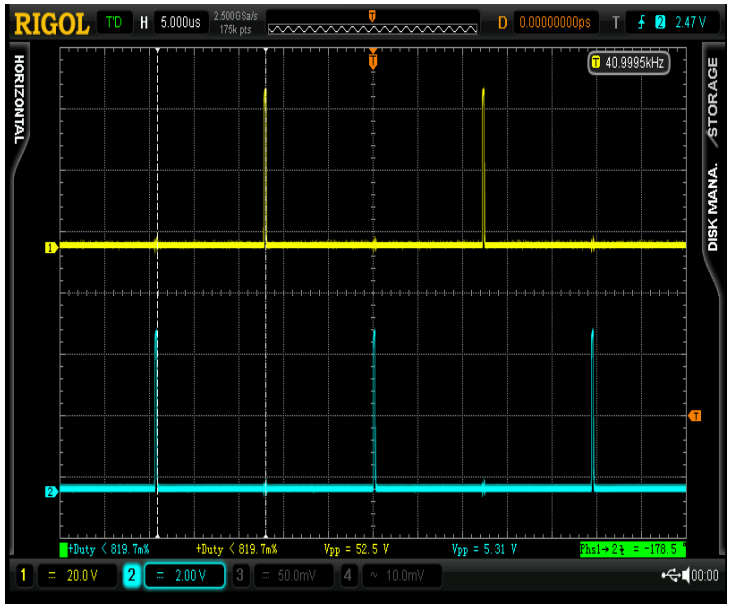
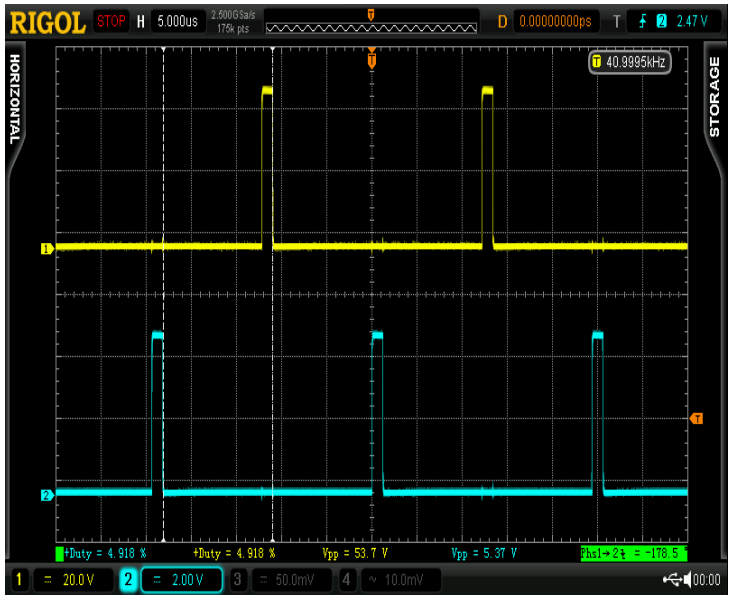
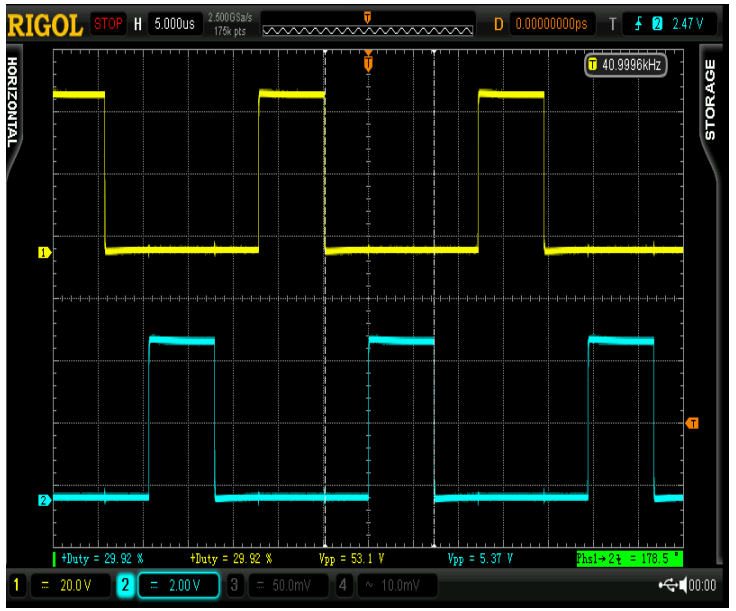
Measurement results: Terminal Voltage Control



Frequency : 41 KHz
Duty Cycle: 1%
Phase difference: 180^o



Frequency : 41 KHz
Duty Cycle: 5%
Phase difference: 180^o



Frequency : 41 KHz
Duty Cycle: 30%
Phase difference: 180^o

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Advantage & Disadvantages

- Advantages
  - Integration to other Tandentron accelerators
  - Repair and upgrade
  - Automated measurement (Quality factor measurement)
- Disadvantages
  - Steep learning curve with FPGA coding
  - External interfacing PCB
  - Accelerator availability for testing

Project status and update

Project Step	Item	Status	Date to be completed
PLC Software development	Frequency Synthesiser	✓	April
	H-Bridge driver	✓	May
	Terminal Voltage control	60%	June
	Interlock	50%	June
Hardware Development	Signal Conditioning	✓	May
	Interface board	60%	June
Testing	Full 2 MV on terminal	30%	July

Special Thanks

- Matthew Rees
- David Button
- Andrew Downes
- David Garton

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